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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,911	01/24/2001	Lap-Wai Chow	B-3962 618027-2	5023

7590 06/02/2003

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EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/768,911	CHOW ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *9-16 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/24/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/21/03 was filed after the mailing date of the Notice of Allowance on 12/18/02. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Allowable Subject Matter

Applicant is advised that the Notice of Allowance mailed 12/18/02 is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

The indicated allowability of claims 1-8, 17 and 19-21 is withdrawn in view of the newly discovered references to Kano, JP 61-147551, and Kowalski, WO 98/57373, both cited in an IDS submitted after the Notice of Allowance was mailed. Rejections based on the newly cited reference(s) follow.

Claim Rej ctions - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kowalski, WO 98/57373.

Kowalski teaches an integrated circuit whose integrity is protected comprising:

(a) an insulating layer (13) disposed on a substrate (11)

(b) a 1st metal layer (14) and a 2nd metal layer (12-2), said 1st and 2nd metal layers being separated by the insulating layer (13); and

(c) a via (V2) defined by said insulating layer, said via having a 1st and 2nd end, wherein said 1st end of said via is connected to said 1st metal layer and said 2nd end of said via terminates prior to reaching the 2nd metal layer.

Regarding claim 2, the device taught by Kowalski is an integrated circuit.

With respect to claim 3, Kowalski teaches the insulating layer to be a silicon dioxide (page 7, lines 9+).

As to claim 20, Kowalski teaches the 1st metal layer is the upper layer and the 2nd metal layer is the lower layer.

Claim 5-7 and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kowalski, WO 98/57373.

Kowalski teaches an integrated circuit whose integrity is protected comprising:

(a) an insulating layer (13) disposed on a substrate (11)

(b) a 1st metal layer (12-2) and a 2nd metal layer (14), said 1st and 2nd metal layers being separated by the insulating layer (13); and

(c) a via (V2) defined by said insulating layer, said via having a 1st and 2nd end, wherein said 2nd end of said via is connected to said 2nd metal layer and said 1st end of said via terminates prior to reaching the 1st metal layer (Figure 2).

Regarding claim 6, the device taught by Kowalski is an integrated circuit.

With respect to claim 7, Kowalski teaches the insulating layer to be a silicon dioxide (page 7, lines 9+).

As to claim 21, Kowalski teaches the 1st metal layer is the lower layer and the 2nd metal layer is the upper layer.

Claims 1, 2, 17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kano, JP 61-147551.

Kano teaches a device that prevents the imitation and copying of a wiring pattern comprising:

(a) an insulating layer (4) disposed on a substrate (1);

(b) a 1st metal layer (7a) and a 2nd metal layer (3c), said 1st and 2nd metal layers being separated by the insulating layer (24); and

(c) a via (6a and/or 6b) defined by said insulating layer, said via having a 1st and 2nd end, wherein said 1st end of said via is connected to said 1st metal layer and said 2nd end of said via terminates prior to reaching the 2nd metal layer.

Regarding claim 2, the device taught by Kano is an integrated circuit.

As to claim 20, Kano teaches the 1st metal layer is the upper layer and the 2nd metal layer is the lower layer.

Claims 5, 6 and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kano, JP 61-147551.

Kano teaches a device that prevents the imitation and copying of a wiring pattern comprising:

(a) an insulating layer (4) disposed on a substrate (1);

(b) a 1st metal layer (7a) and a 2nd metal layer (3c), said 1st and 2nd metal layers being separated by the insulating layer (24); and

(c) a via (6a and/or 6b) defined by said insulating layer, said via having a 1st and 2nd end, wherein said 1st end of said via is connected to said 1st metal layer and said 2nd end of said via terminates prior to reaching the 2nd metal layer.

Regarding claim 6, the device taught by Kano is an integrated circuit.

As to claim 21, Kano teaches the 1st metal layer is the lower layer and the 2nd metal layer is the upper layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kowalski, WO 98/57373 as applied to claims 1 and 5 above respectively, and further in view of Wolf, Silicon Processing for the VLSI Era-Volume 2:Process Integration, Lattice Press, 1990, pp. 387, 482 and 508.

Kowalski fails to teach the integrated circuit (IC) being a CMOS, bipolar silicon or III-V integrated circuit.

Wolf teaches the use of a CMOS IC (p. 384), a bipolar Si IC (p.482) and a GaP (III-V) IC as being conventionally known in the art substrates.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 3, 4, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kowalski, WO 98/57373 as applied to claims 1 and 5 above respectively, and further in view of Wolf, Silicon Processing for the VLSI Era-Volume 2:Process Integration, Lattice Press, 1990, pp. 194-199, 387, 482 and 508.

Regarding claims 3 and 7, Kano fails to teach a specific insulating material, let alone the use of silicon oxide as the insulating material.

Wolf (pp. 194-199) teaches the use of silicon oxides as a conventionally known in the art intermetal dielectric.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

With respect to claims 4 and 8, Kano fails to teach the integrated circuit (IC) being a CMOS, bipolar silicon or III-V integrated circuit.

Wolf (pp. 387, 482 and 508) teaches the use of a CMOS IC (p. 384), a bipolar Si IC (p.482) and a GaP (III-V) IC (p. 508) as being conventionally known in the art IC substrates.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
April 10, 2003